Sree Charan Gundabolu

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Education

Purdue University — West Lafayette, IN
Doctor of Philosophy in Computer Engineering; ***GPA: 3.57*** *Aug. 2018 – Present*

Villanova University — Philadelphia, PA
Master of Science in Computer Engineering; ***GPA: 3.95*** *Jan. 2016 – May 2018*

Reva Institute of Technology and Management — Bangalore, India
Bachelor of Engineering in Electronics and Communication; ***GPA: 7.7/10.0*** *Aug. 2011 – June. 2015*

Relevant Coursework

Machine Learning	Artificial Intelligence	Linear Algebra
Design and Analysis of Algorithms	Probability	Data Structures Using C++
Computer Architecture	Embedded System Design	Trusted Computing
Microprocessors & Microcomputers	Unix and C Programming	Compilers and Translation Engineering
ML in Bioinformatics	Operating Systems	Programmable Accelerator Architectures

Experience

Research Assistant — **Advisors: Dr.Mithuna Thottethodi & Dr.T. N. Vijaykumar**
Purdue University *Aug 2018 - Present*

Research Project 2
- Enhanced the performance of BLASTP, a protein sequence search tool, by identifying bottlenecks in its pipeline and implementing GPU-accelerated parallel algorithms.
- Achieved significant speed improvements, accelerating various stages of the application and resulting in a faster end-to-end protein sequence analysis tool.

Research Project 1
- Designed and implemented a GPU kernel to perform efficient Gapped Whole Genome Alignment(WGA) using CUDA to accelerate the slow dynamic programming based Gotoh algorithm on GPUs with application specific optimizations for Gapped WGA.
- The kernel performed 111x faster than sequential iso software on an NVIDIA Ampere GPU.

Teaching Assistant — **Dr.Mithuna Thottethodi & Dr.Phillip Walter**
Purdue University *Aug 2020 - Aug 2021*

- Assisted student groups with their senior design CompE projects. Work closely with teams to assist them through the entire design process, including determining project-specific success goals, selecting components, prototyping, PCB design, and packaging.
- Collaborated with other teaching assistants to document the course logistics to create a staff survival guide for future course staff.

Research Assistant — **Advisor: Dr.Xiaofang Wang**
Villanova University *Jan 2017 - May 2018*

Research Project 2
- Designed and implemented a hybrid hardware-software based monitor to protect data in distributed on-chip memory in FPGAs. The main responsibility of the monitor was to enforce access policy in a shared environment, consisting of hardware and software intellectual properties(IPs) designed in-house and obtained from untrusted 3rd party vendors.

Research Project 1
- Designed and implemented a weighted voting based technique to enhance the efficiency of the commonly used triple redundancy design. This enabled detection of malicious 3rd party IPs and mitigate their effects in critical applications. The design was tested on a Xilinx Zedboard FPGA (Vivado ISE) validated using Trojan benchmarks from (trust-hub.org).

Teaching Assistant — **Dr.Xiaofang Wang, Dr.Edward Hepler, Dr.Edward Kresch**
Villanova University *Jan 2017 - May 2018*

- Assisted in designing and testing a new 6-lab curriculum to implement single-cycle and pipelined versions of MIPS processors for an undergraduate Computer Architecture course.
- Tutored students and assisted them in labs.

Projects

- **Adversarial Machine Learning:** Implemented Fast Gradient Sign method, Projected Gradient Descent, Carlini and Wagner attack, and Deepfool attack on a classifier trained to classify digits from the MNIST database. Mitigating strategies namely, Denoising Autoencoders, Adversarial Training, Dimensionality Reduction, and Adversarial Detection were studied and implemented in python using Keras.
- **PetBuddy:** Designed and prototyped an autonomous robot to find a pet in an apartment, while a smartphone application allowed users to view a live stream and dispense pet treats. PetBuddy used a PiCamera interfaced with a NVIDIA Jetson Nano to run real-time inference on a YOLOv2 network to detect pets. Stepper motors were used to actuate the pet feeders, and the pet toys; a laser light for cats and a ball launcher for dogs. Amazon AWS ran a web server to provide a live stream, SWIFT was used to develop an iOS and Android app.
- **CUDA Software Programming:** Implemented SAXPY and Median filtering kernels with various optimizations and compared their performance on the GPU. Implemented the AlexNet network to perform object detection from scratch, by implementing efficient CUDA kernels to perform, max pooling, convolution, and efficient General Matrix Multiply (GEMM).
- **GPU Architecture:** Compare and contrast the execution of PTX vs SASS generated code on the trace-based GPU simulator Accel-Sim. Modify GPGPU-sim to support multiple CTA-scheduling strategies to allocate blocks to SMs, including flat scheduling, greedy, and round-robin scheduling. Implemented many thread-aware prefetch mechanisms, and measured the performance improvement by comparing the relative IPC, cache misses, and the number of prefetch hits.
- **Compiler and Translator Systems:** Designed and Implemented a compiler to compile a C program into RISC-V assembly. This included programming a scanner, parser, and a code generator, using Java. The compiler supported programming features such as arrays, pointers, control structures, functions, recursive data structures, typecasting and checking. The compiler-generated machine code with the following optimizations, a program stack, register allocation, memory allocation on the heap, and global liveness and dead code elimination.
- **Advance computer systems:** Implemented Adaptive Selective Replication(ASR) for Chip Multiprocessors(CMP) to adaptively replicate cache blocks in shared L2 and private caches to minimize off-chip misses. ASR was implemented on gem5 and its performance was evaluated and verified using commercial and scientific workloads as specified in the original research paper.
- **Learning-Based Sequence Alignment:** Reviewed research on enhancing sequence alignment through structural information, highlighting the potential of Alphafold2's 3D protein structures for superior alignments compared to traditional methods.

Publications

- **Sree Charan Gundabolu**, T. N. Vijaykumar, and Mithuna Thottethodi. 2021. FastZ: accelerating gapped whole genome alignment on GPUs. In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (SC '21).
- Ashish Gondimalla, **Sree Charan Gundabolu**, T. N. Vijaykumar and Mithuna Thottethodi. 2021. Barrier-Free Large-Scale Sparse Tensor Accelerator (BARISTA) For Convolutional Neural Networks. Computing Research Repository (CoRR).
- **S. Gundabolu** and X. Wang, 2018. On-chip Data Security Against Untrustworthy Software and Hardware IPs in Embedded Systems. IEEE Computer Society Annual Symposium on VLSI (ISVLSI).

Skills

- **Tools** TensorFlow, PyTorch, Keras, Numpy, Pandas, AWS, MySQL, Keil MATLAB/Octave, LabView, EAGLE, KiCad.
- **Programming Languages** Python, C, C++, Verilog, VHDL, Java, Assembly level language, LaTeX